REMARKS

Claims 1-20 are pending in the application. Claims 9-20 were withdrawn from consideration as being drawn to non-elected subject matter. Claim 1 has been amended by the present amendment. The amendment is fully supported by the application as originally filed (see, e.g., page 8, last paragraph to page 9, first paragraph; FIGS. 1 and 2C).

As amended, claim 1 recites a semiconductor package in which a chip and conductive bumps are completely encapsulated by a **single** encapsulation body, and a plurality of conductive traces are formed at the surface of the encapsulation body exposing the conductive bumps, the conductive traces being electrically connected to exposed ends of the conductive bumps.

For example, referring to FIGS. 1 and 2C, the encapsulation body 22 completely encapsulates the chip 20 and conductive bumps 21. In other words, the encapsulation body 22 is a **single** encapsulation body for encapsulating all of the chips 20 and conductive bumps 21 (see page 8, last paragraph to page 9, first paragraph). As shown in FIG. 1, conductive traces 23 are formed at the surface of the encapsulation body on exposed ends of the conductive bumps 21.

Claims 1, 2, and 5-8 were rejected under 35 USC 102(e) as being anticipated by U.S. Patent 6,701,614 to Ding et al. ("Ding"). Claims 3 and 4 were rejected under 35 USC 103(a) as being unpatentable over Ding in view of U.S. Patent 6,734,534 to Vu et al. ("Vu"). These rejections are respectfully traversed.

Ding does not teach or suggest a semiconductor package in which a chip and conductive bumps are completely encapsulated by a **single** encapsulation body, and a plurality of conductive traces are formed at the surface of the encapsulation body exposing the conductive bumps, as recited in claim 1.

Referring to FIG. 4h of Ding, as cited in the Final Office Action, die 30 is encapsulated by an encapsulating material 40 (see column 5, lines 53-55). A first dielectric layer 61 is formed on a surface of the encapsulating material 40 (see column 5, lines 57-59).

In the Final Office Action, the encapsulating material 40 and the first dielectric layer 61 of Ding were cited as corresponding to Applicants' claimed "encapsulation body."

However, the encapsulating material 40 and first dielectric layer 61 do not constitute a **single** encapsulation body for completely encapsulating a chip and conductive bumps. Moreover, in Ding, the conductive traces 72 are formed on the first dielectric layer 61, not at the surface of an encapsulation body exposing the conductive bumps.

For at least the reasons discussed above, the Ding reference does not anticipate or otherwise render obvious the Applicants' claimed invention.

It is believed the application is in condition for immediate allowance, which action is earnestly solicited.

Respectfully submitted,

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